PTO/SB/17 (12-04v2)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Effective on 12/08/2004.
Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL
For FY 2005

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT	($)	500.00

Complete If Known	
Application Number	09/712,873
Filing Date	15 Nov. 2000
First Named Inventor	Krinder, Jason D.
Examiner Name	2134
Art Unit	Nalven, Andrew L.
Attorney Docket No.	TI-29077

METHOD OF PAYMENT (check all that apply)

☐ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☑ Deposit Account Deposit Account Number: 20-0668 Deposit Account Name: Texas Instruments

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☑ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, except for the filing fee

☑ Charge any additional fee(s) or underpayments of fee(s) under 37 CFR 1.16 and 1.17 ☑ Credit any overpayments

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FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

Application Type	FILING FEES Fee ($)	FILING FEES Small Entity Fee ($)	SEARCH FEES Fee ($)	SEARCH FEES Small Entity Fee ($)	EXAMINATION FEES Fee ($)	EXAMINATION FEES Small Entity Fee ($)	Fees Paid ($)
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

28

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 (including Reissues)	50	25
Each independent claim over 3 (including Reissues)	200	100
Multiple dependent claims	360	180

Total Claims	Extra Claims	Fee ($)	Fee Paid ($)
_____ - 20 or HP =	_____	x _____	= _____

HP = highest number of total claims paid for, if greater than 20.

Indep. Claims	Extra Claims	Fee ($)	Fee Paid ($)
_____ - 3 or HP =	_____	x _____	= _____

HP = highest number of independent claims paid for, if greater than 3.

Multiple Dependent Claims Fee ($)	Multiple Dependent Claims Fee Paid ($)
_____	_____

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(c)), the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee ($)	Fee Paid ($)
_____ - 100 =	_____	/ 50 = _____ (round up to a whole number)	x _____	= _____

4. OTHER FEE(S)

	Fees Paid ($)
Non-English Specification. $130 fee (no small entity discount)	
Other (e.g., late filing surcharge): Filing a brief in support of an appeal	500.00

SUBMITTED BY

Signature		Registration No. (Attorney/Agent) 46,723	Telephone (512) 899 4732
Name (Print/Type)	Georgios A. Georgakis		Date January 3, 2006

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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Total Number of Pages in This Submission: 18

Application Number	09/712,873
Filing Date	15 November, 2000
First Named Inventor	Krinder, Jason D.
Art Unit	2134
Examiner Name	Nalven, Andrew L.
Attorney Docket Number	TI-29077

ENCLOSURES (Check all that apply)

- [✔] Fee Transmittal Form
  - [ ] Fee Attached
- [ ] Amendment/Reply
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Reply to Missing Parts/ Incomplete Application
  - [ ] Reply to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing related Papers
- [ ] Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s) _____
  - [ ] Landscape Table on CD
- [ ] After Allowance Communication to TC
- [ ] Appeal Communication to Board of Appeals and Interferences
- [✔] Appeal Communication to TC (Appeal Notice, Brief, Reply Brief)
- [ ] Proprietary Information
- [ ] Status Letter
- [ ] Other Enclosure(s) (please identify below):

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	Chowdhury & Georgakis		
Signature			
Printed name	Georgios A. Georgakis		
Date	January 3, 2006	Reg. No.	46,723

CERTIFICATE OF TRANSMISSION/MAILING

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Typed or printed name	Georgios A. Georgakis	Date	January 3, 2006

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:		Docket No.:	TI-29077
	Jason D. Krinder	Art Unit:	2134
Serial No:	09/712,873	Examiner:	Nalven, Andrew L.
Filed:	November 15, 2000	Conf. No.:	9315
For:	Authorization Control Circuit and Method		

January 3, 2006

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on January 3, 2006.

Georgios A. Georgakis, Reg. No. 46,723

APPEAL BRIEF

Dear Sir:

Applicant respectfully appeals the decision of the Examiner to finally-reject Claims 1–23, as set forth in the final Office Action of June 29, 2005.

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(I) REAL PARTY IN INTEREST

The Real Party in Interest in this matter is Texas Instruments Incorporated, the assignee.

(II) RELATED APPEALS AND INTERFERENCES

Applicant is unaware of any related appeals or interferences pertaining to this matter.

(III) STATUS OF CLAIMS

Claims 1-23 are currently pending in this application. The Examiner issued a Final Rejection of Claims 1-23 on June 29, 2005. Claims 1-23 are the subject of this appeal.

(IV) STATUS OF AMENDMENTS

All amendments have been entered.

(V) SUMMARY OF CLAIMED SUBJECT MATTER

The present invention relates to an authorization control circuit in an electronic device, comprising:

a digital signal processor operable to provide digital data output, determine an authorization state, and generate a disable signal;

a digital to analog converter coupled to the digital signal processor and operable to receive the digital data output, convert the digital data to corresponding analog data, output the corresponding analog data, and mute the output of the corresponding analog data; and

the converter including an input operable to receive the disable signal, and the converter muting the output of the corresponding analog data in response to the disable signal, wherein the disable signal is generated when the electronic device satisfies one or more sleep conditions.

The present invention also relates to an authorization control circuit in an electronic device, comprising:

a digital signal processor operable to provide digital data output, determine an authorization state, and generate a disable signal;

a digital to analog converter coupled to the digital signal processor and operable to receive the digital data output, convert the digital data to corresponding analog data, and output the corresponding analog data; and

an analog amplifier operable to receive the analog output from the converter and generate amplified output, and having an input operable to receive the disable signal, the amplifier muting the amplified output in response to the disable signal, wherein the disable signal is generated when the electronic device satisfies one or more sleep conditions.

The present invention further relates to a method of selectively muting output, comprising the steps of:

generating digital data;

determining an authorization state, wherein determining the authorization state comprises comparing a mathematical function result to an expected result;

generating a disable signal;

transmitting the digital data to a digital to analog converter;

generating an analog signal corresponding to the digital data;

transmitting the disable signal to the digital to analog converter; and

muting the analog signal in response to the transmitted disable signal.

(VI) GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether Claims 1–23 are not obvious under 35 U.S.C. 103(a) over DeLuca et al (US Patent No 5,612,682) in view of Seo et al (US Patent No 5,063,597), Tran (US Patent No. 5,734,729), and Nagata (US Patent No. 6,114,981) and therefore patentable.

(VII) ARGUMENT

The Rejection of Claim 1 under 35 U.S.C. 103(a)

1) Summary of the Rejection:

The Examiner rejected Claim 1 under 35 U.S.C. 103(a) as being unpatentable over DeLuca in view of Seo, Tran, and Nagata.

2) The References cited by The Examiner:

For purposes of providing background, Applicant briefly discusses the DeLuca, Seo, Tran, and Nagata references cited by the Examiner. DeLuca discloses methods for controlling utilization of a process added to a communications device. Seo teaches a muting circuit in a digital audio system. Tran teaches a disable signal generated when an

electronic device satisfies one or more sleep conditions, and Nagata teaches a D/A converter.

3) The Present Invention:

Claim 1 teaches an authorization control circuit in an electronic device, comprising:

a digital signal processor operable to provide digital data output, determine an authorization state, and generate a disable signal;

a digital to analog converter coupled to the digital signal processor and operable to receive the digital data output, convert the digital data to corresponding analog data, output the corresponding analog data, and mute the output of the corresponding analog data; and

the converter including an input operable to receive the disable signal, and the converter muting the output of the corresponding analog data in response to the disable signal, wherein the disable signal is generated when the electronic device satisfies one or more sleep conditions.

4) Arguments:

The Examiner has not established a prima facie case of obviousness. MPEP 2143 states:

To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined)

must teach or suggest all the claim limitations. The Applicant respectfully submits that the Examiner has failed to meet these basic criteria and has therefore failed to make a prima facie case of obviousness. These criteria are discussed below.

First, regarding the requirement that there must be some suggestion or motivation to modify the reference or to combine reference teachings, the Applicant respectfully submits that the Examiner has shown no such suggestion or motivation. In fact, the Examiner introduces reference teachings that teach away from the teachings of Claim 1. The Examiner mistakenly states that Seo teaches a digital-to-analog converter ... operable to ... mute the output of a corresponding analog data in response to a disable signal (see page 3 of Final Rejection). Seo actually teaches a first switching circuit that receives a mute control and a first digital data from a DSP and a fourth digital data from a multiplier. The first switching circuit then selects and outputs selectively the first or the fourth digital data to a digital-to-analog converter (Seo column 3, lines 32-38). The Applicant respectfully submits that the Examiner mistakenly states that the digital-to-analog converter receives the disable signal and mutes the output of the corresponding analog data in response thereto. It is the first switching circuit that receives the mute signal, not the digital-to-analog converter. Seo specifically teaches not to output the disable or mute signal to a digital-to-analog converter. Therefore, Seo teaches away from what the Applicant claims as the invention and away from combining the references as was suggested by the Examiner.

Correspondingly, Seo also teaches away from additional teachings of Claim 1. Claim 1 further teaches the converter muting the output of the corresponding analog data in response to the disable signal. Seo specifically teaches not to output the disable or

mute signal to a digital-to-analog converter and thus teaches away from what the Applicant claims as the invention. Thus, the first criterion of MPEP 2143 is not met.

Second, the Applicant submits that the references do not teach or suggest all of the claim limitations. For example, the Examiner asserts that Seo discloses a digital to analog converter ... operable to ... mute the output of the corresponding analog data. As described above, Seo actually teaches a first switching circuit that receives a mute control and a first digital data from a DSP and a fourth digital data from a multiplier. The first switching circuit then selects and outputs selectively the first or the fourth digital data to a digital-to-analog converter (Seo, Column 3, Lines 32-38). The Applicant respectfully submits that the Examiner mistakenly states that the digital-to-analog converter receives the disable signal and mutes the output of the corresponding analog data in response thereto. It is the first switching circuit that receives the mute signal, not the digital-to-analog converter. Thus, the references do not teach or suggest all of the claim limitations, and the second criterion of MPEP 2143 is not met.

Finally, as for the remaining criterion of MPEP 2143, the reasonable expectation of success, the Applicant submits that the absence of the recited claim limitations and the presence of references which teach away from the present invention preclude any reasonable expectation of success. Consequently, this criterion is also not met by the Examiner.

Since the Examiner has failed to meet the three criteria of MPEP 2143, the Examiner has failed to make a prima facie case of obviousness. The rejection of Claim 1 under 35 U.S.C.103(a) in view of DeLuca, Seo, Tran, and Nagata is therefore

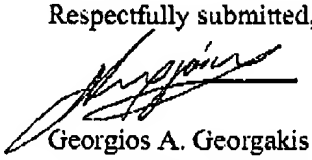
improper. For at least the reasons stated above with respect to Claim 1, the rejection of independent Claims 9 and 12 and dependent Claims 10, 11, and 13-20 is also improper.

Conclusion

For the reasons set forth above, Applicant respectfully submits that Claims 1-23 are patentable over DeLuca, Seo, Tran, and Nagata. Accordingly, Applicant prays that this Honorable Board will reverse the Primary Examiner's rejection of Claims 1-23.

The Commissioner is authorized to charge the $500.00 appeal brief fee and any other fees associated with this appeal brief to Deposit Account 20-0668 of Texas Instruments Incorporated.

Respectfully submitted,



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(VIII) CLAIMS APPENDIX

Reprinted below are the claims involved in this appeal:

1. An authorization control circuit in an electronic device, comprising:

a digital signal processor operable to provide digital data output, determine an authorization state, and generate a disable signal;

a digital to analog converter coupled to the digital signal processor and operable to receive the digital data output, convert the digital data to corresponding analog data, output the corresponding analog data, and mute the output of the corresponding analog data; and

the converter including an input operable to receive the disable signal, and the converter muting the output of the corresponding analog data in response to the disable signal, wherein the disable signal is generated when the electronic device satisfies one or more sleep conditions.

2. The circuit of Claim 1, wherein the authorization state is either positive or negative and the digital signal processor is operable to generate the disable signal when the authorization state is negative.

3. The circuit of Claim 1, the converter further comprising a serial input for receiving timing signals to enable reception of the disable signal.

4. The circuit of Claim 1, wherein the analog output is muted by filtering the received digital data prior to conversion into analog data.

5. The circuit of Claim 1, the digital signal processor further comprising:

an output pin operable to transmit the disable signal as a high voltage.

6. The circuit of Claim 1, the converter further comprising:

a pull-down circuit operable to create a low voltage at the input in the absence of a disable signal.

7. The circuit of Claim 1, wherein the authorization state is either positive or negative and the digital signal processor is not operable to generate the disable signal when the authorization state is negative.

8. The circuit of Claim 1, wherein the digital signal processor has at least two output pins, the first pin provides a clock signal, the second pin provides the disable signal, and the state of the disable signal at the rising edges of the clock signal are read by the converter.

9. An authorization control circuit in an electronic device, comprising:

a digital signal processor operable to provide digital data output, determine an authorization state, and generate a disable signal;

a digital to analog converter coupled to the digital signal processor and operable to receive the digital data output, convert the digital data to corresponding analog data, and output the corresponding analog data; and

an analog amplifier operable to receive the analog output from the converter and generate amplified output, and having an input operable to receive the disable signal, the amplifier muting the amplified output in response to the disable signal, wherein the disable signal is generated when the electronic device satisfies one or more sleep conditions.

10. The circuit of Claim 9, wherein the authorization state is either positive or negative and the digital signal processor is operable to generate the disable signal when the authorization state is negative.

11. The circuit of Claim 9, wherein the authorization state is either positive or negative and the digital signal processor is not operable to generate the disable signal when the authorization state is negative.

12. A method of selectively muting output, comprising the steps of:

generating digital data;

determining an authorization state, wherein determining the authorization state comprises comparing a mathematical function result to an expected result;

generating a disable signal;

transmitting the digital data to a digital to analog converter;

generating an analog signal corresponding to the digital data;

transmitting the disable signal to the digital to analog converter; and

muting the analog signal in response to the transmitted disable signal.

13. The method of Claim 12, wherein the step of muting comprises activating a digital filter.

14. The method of Claim 12, wherein the step of muting comprises signal processing that occurs after the step of generating the analog signal.

15. The method of Claim 12, wherein the authorization state is either positive or negative and the disable signal is generated after the authorization state is determined to be negative.

16. The method of Claim 12, further comprising the step of:

generating a clock signal and wherein the step of muting is in response to the state of the disable signal at the rising edges of the clock signal.

17. The method of Claim 16, wherein the clock signal is transmitted contemporaneously with the disable signal.

18. The method of Claim 12, further comprising the step of:

generating a power-save signal and wherein the disable signal is generated in response to the power-save signal.

19. The method of Claim 12, further comprising the steps of:

generating an override signal; and

terminating the muting step in response to the override signal.

20. The method of Claim 19, further comprising the step of:

detecting the step of generating the disable signal; and wherein the override signal is generated in response to the detection of the disable signal.

21. The circuit of Claim 1, wherein one of the sleep conditions is usage of the electronic device, said disable signal generated when the usage meets a predetermined criteria.

22. The circuit of Claim 1, wherein the electronic device is a music player, video player, or multimedia file player.

23. The method of Claim 12, wherein the step of determining an authorization state further comprises:

selecting a data file, wherein the data file includes the digital data; and

performing a hashing function on the data file to generate the mathematical function result, wherein the hashing function is executed by a digital signal processor.

(IX) EVIDENCE APPENDIX

No additional evidence is submitted.

(X) RELATED PROCEEDINGS APPENDIX

Applicant is unaware of any related appeals or interferences pertaining to this matter.